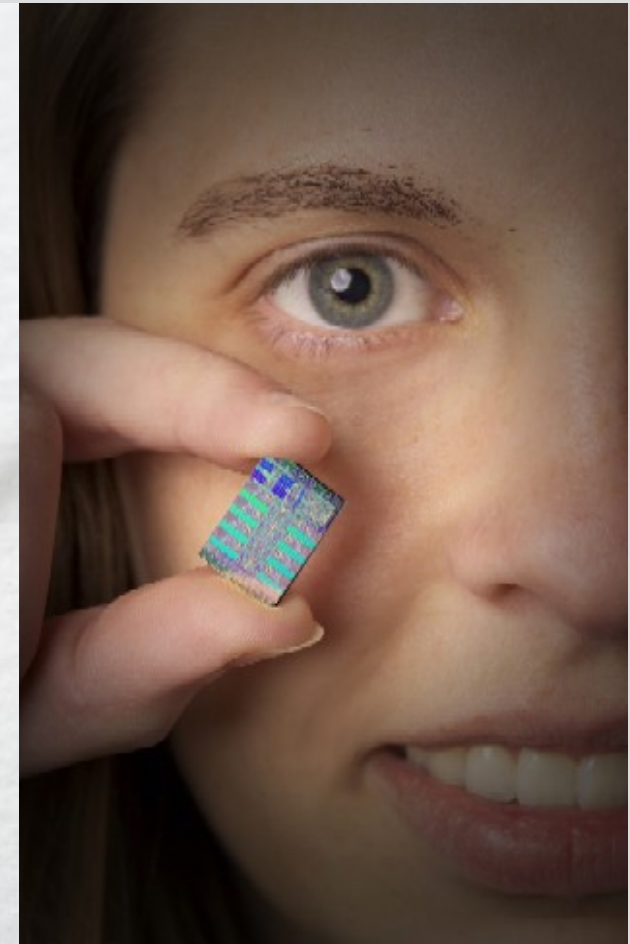
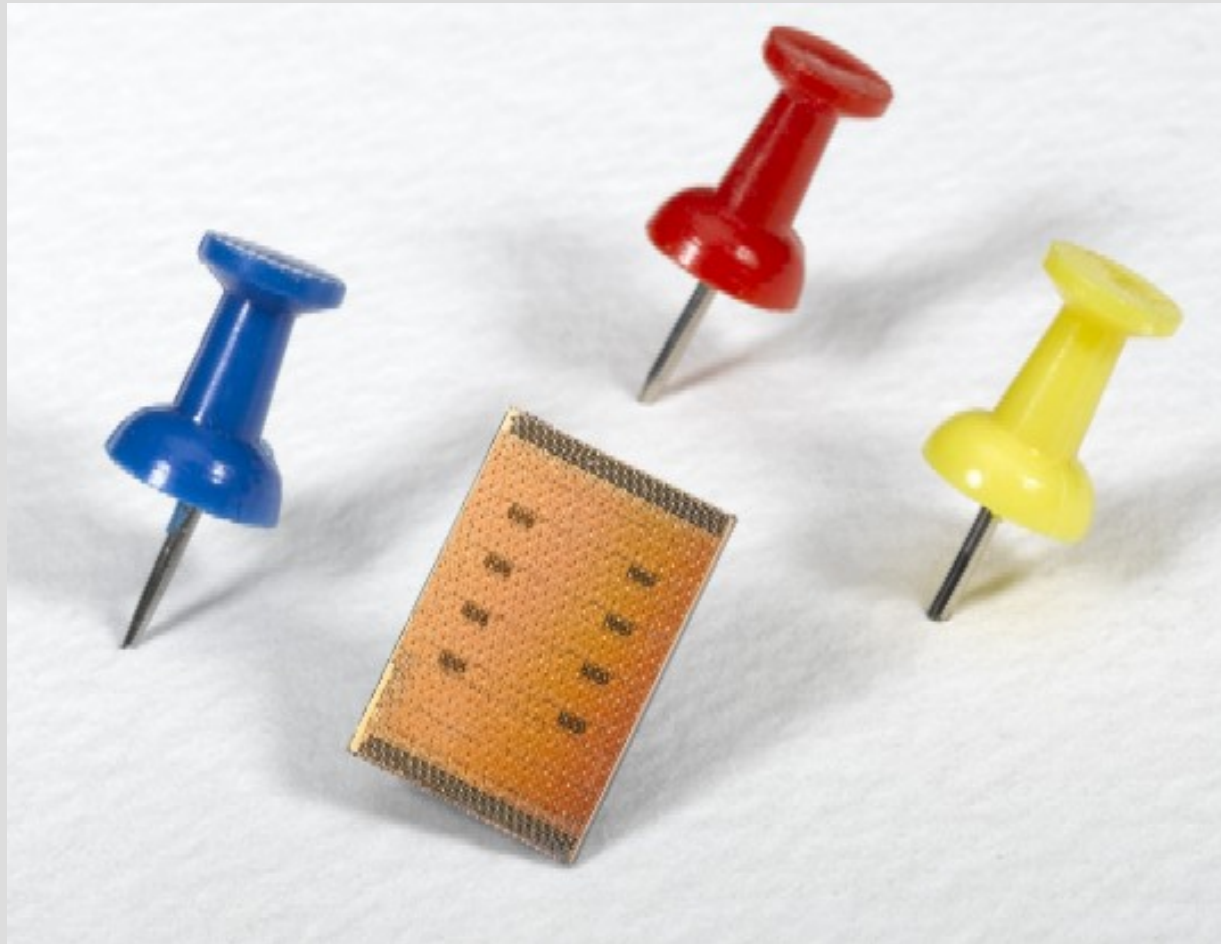


# An Introduction to the “Cell Broadband Engine” Processor & Cell Architecture



Cell BE Resource Center: <http://www.ibm.com/developerworks/power/cell>

Information, graphics, and diagrams courtesy IBM Corporation.

**Trademarks** – Cell Broadband Engine is a trademark of Sony Computer Entertainment, Inc.

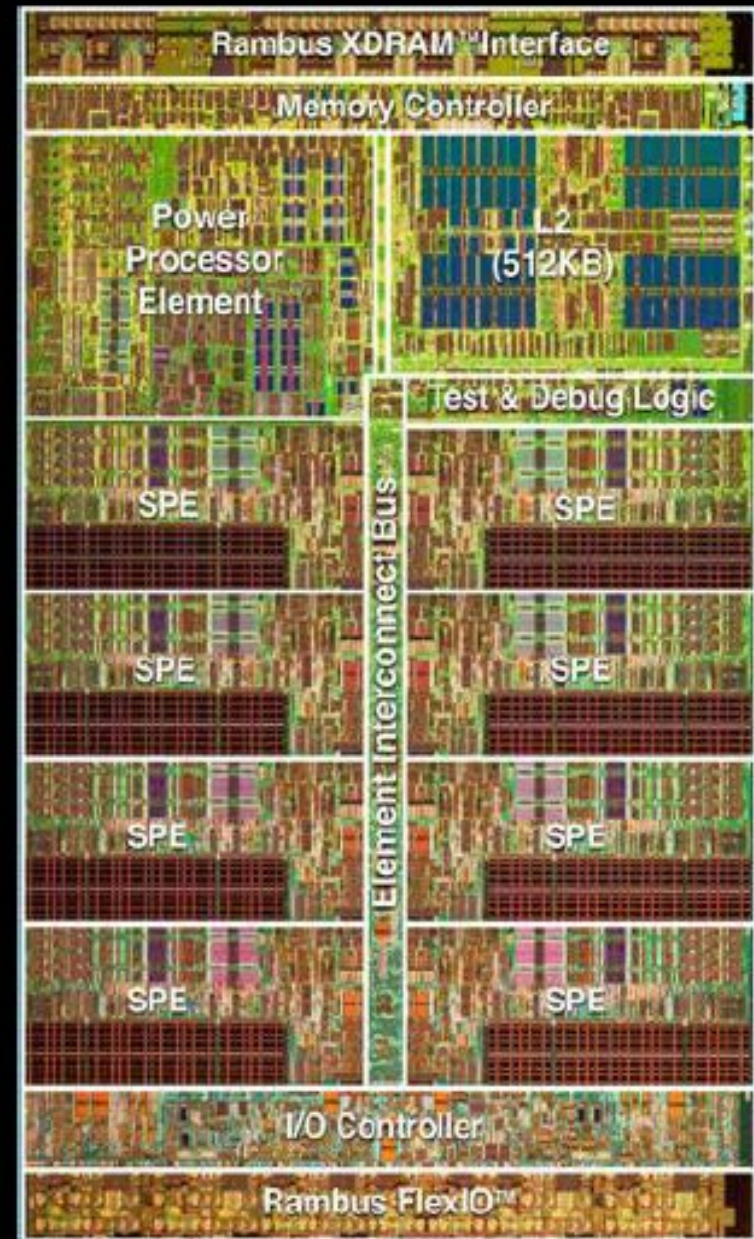
# Cell Development

- Cell Broadband Engine (“Cell”) is the result of a deep partnership between SCEI/Sony, Toshiba, and IBM
- Cell represents the work of more than 400 people starting in 2001 and a design investment of about \$400M



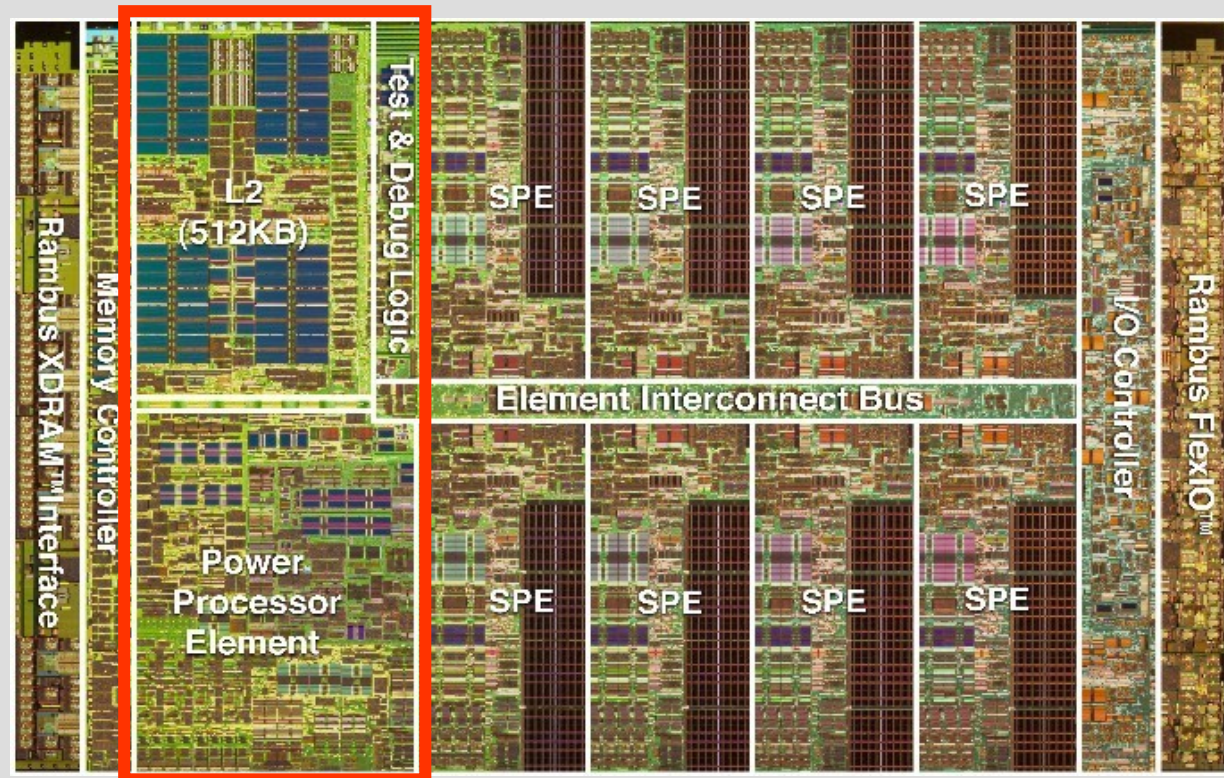
# Highlights (3.2 GHz)

- 241M transistors
- 235mm<sup>2</sup>
- 9 cores, 10 threads
- >200 GFlops (SP)
- >20 GFlops (DP)
- Up to 25 GB/s memory B/W
- Up to 75 GB/s I/O B/W
- >300 GB/s EIB
- Top frequency >4GHz (observed in lab)



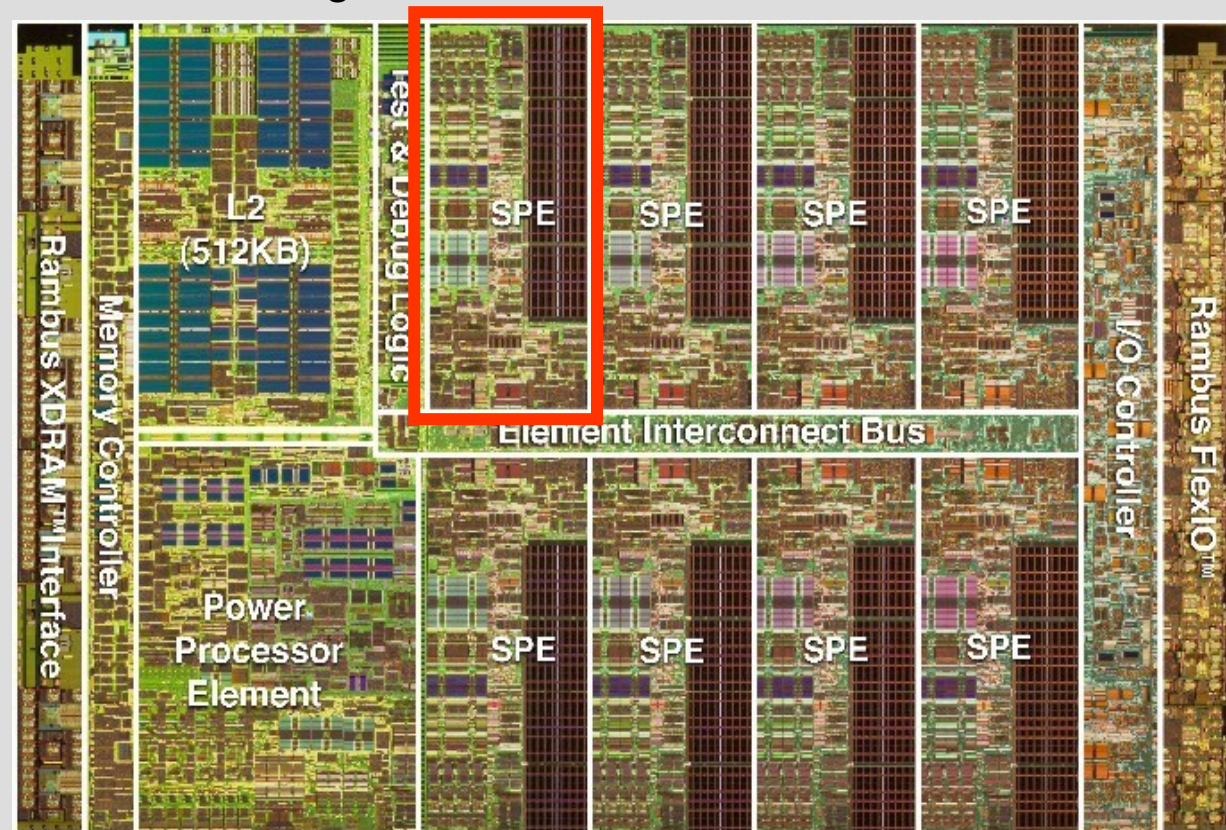
# Power Processor Element (PPE)

- ▶ 64-bit Power Processor (based on the Power PC line)
- ▶ 32KB L1 cache & 512KB L2 cache
- ▶ Runs the operating system (Linux)
- ▶ Performs thread management
- ▶ Mediates interrupts for system



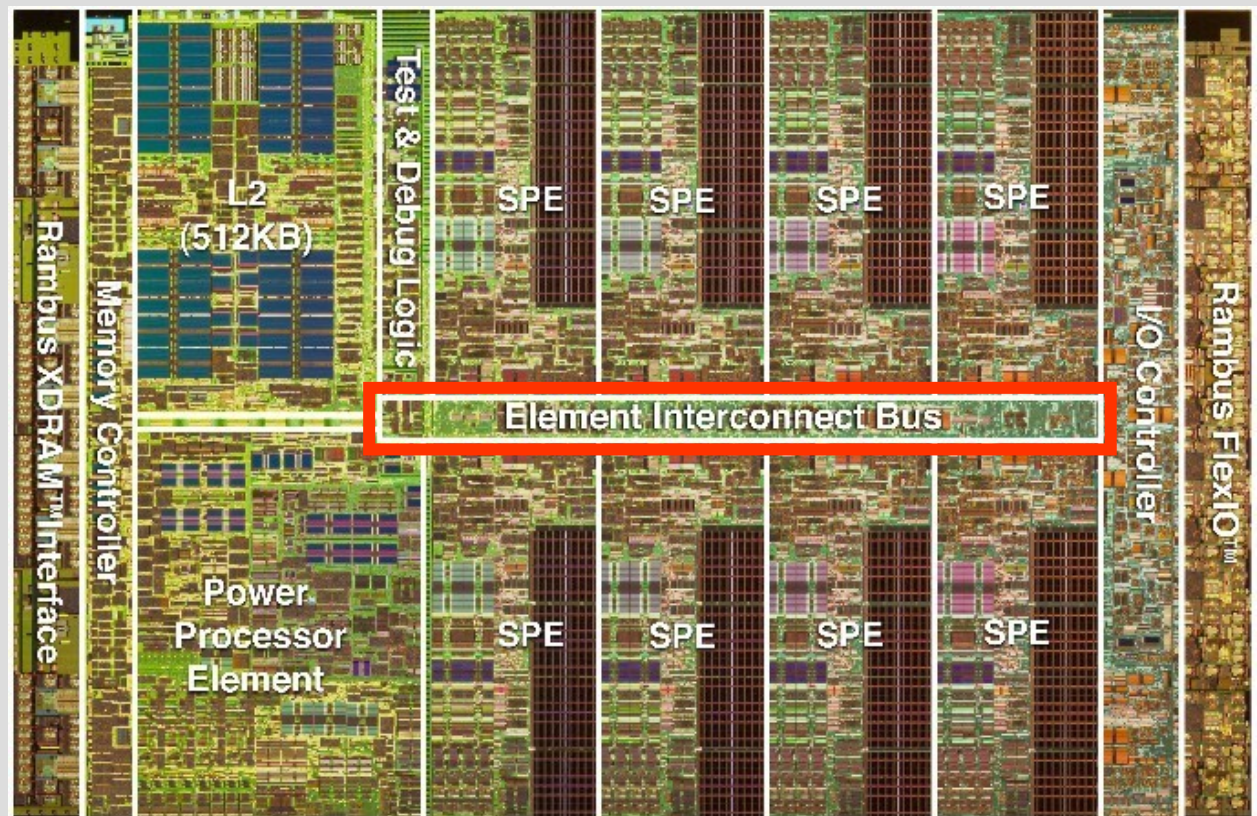
# Synergistic Processor Element (SPE)

- ◆ 8 SPEs per Cell Chip.
- ◆ RISC-like organization
- ◆ 256k Local Store (cache) for both data AND code
- ◆ 128x128b register file.
- ◆ Dedicated DMA engine, up to 16 outstanding requests.



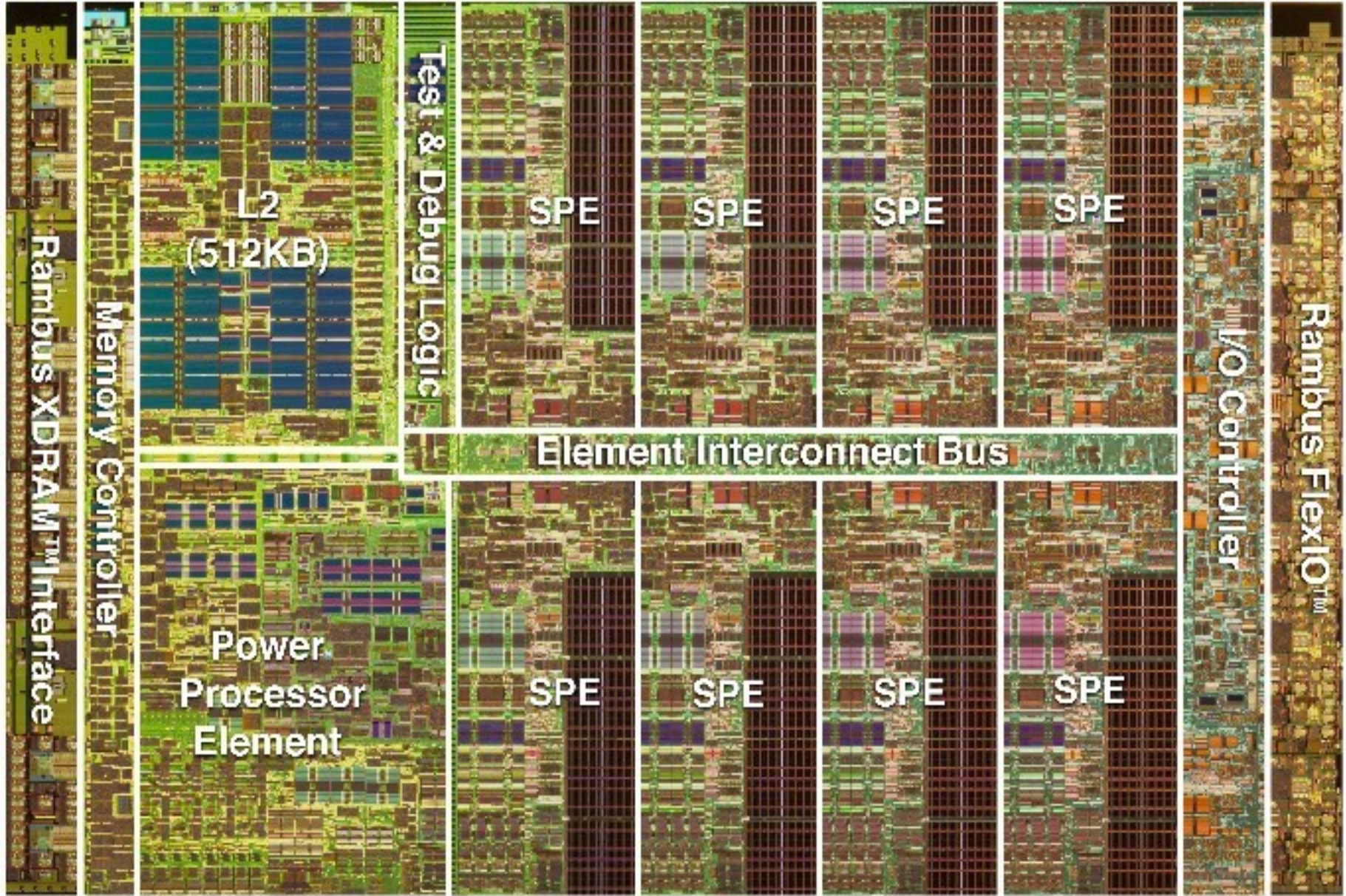
# Element Interconnect Bus (EIB)

- ▶ Four 16 byte data rings, each supporting multiple transfers.
- ▶ 96B/cycle peak bandwidth
- ▶ Over 100 outstanding requests





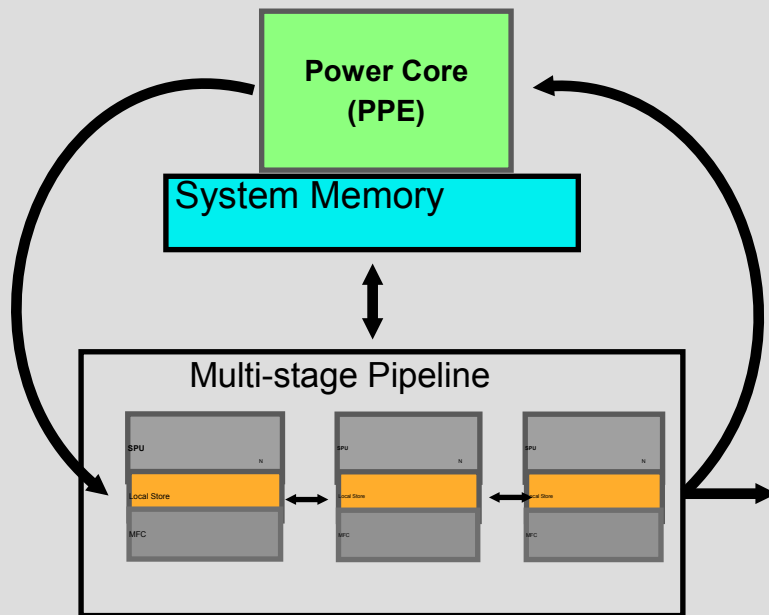
# Cell Broadband Engine



# Programming Models

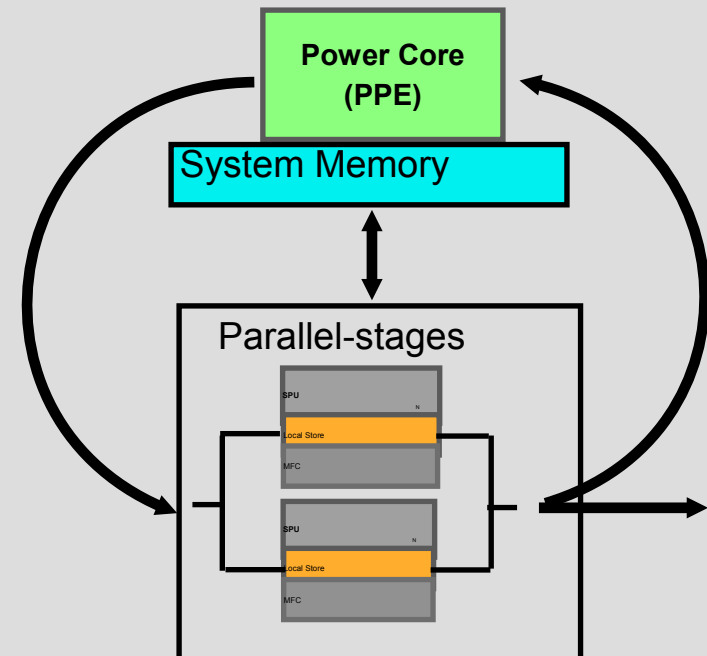
## Multi-Stage Pipeline

- ▶ Data processing that can be performed in segments are divided among SPEs.
- ▶ Example: Digital Video Surveillance



## Parallel-Stages

- ▶ A single algorithm processing a large amount of data.
- ▶ Examples: Matrix multiplication,



# Cell Application Affinity

## Cell Broadband Engine

- Non-homogeneous coherent multi-Processor
  - Dual-threaded control-plane processor
  - 8 independent data-plane processors
  - Thread-level parallelism
- SIMD processing architecture
  - 128-entry, 128-bit register files
  - Pipelined execution units
  - Branch hint
  - Data-level parallelism
- Rich integer instruction set
  - Word, halfword, byte, bit
  - Boolean
  - Shuffle
  - Rotate, shift, mask
- Single-precision floating point
- Double-precision floating point
- 256KB SPU local stores
  - Asynchronous DMA/main memory interface
  - Channel interface
  - Single-cycle load/store to/from registers
- High-bandwidth internal bus
  - 96 bytes transferred per clock
  - 100+ outstanding transfers supported
- Coherent bus interface
  - Up to 30GB/s out, 25 GB/s in
  - Direct attach of another Cell
  - Can be configured as non-coherent
- Non-coherent bus interface
  - Up to 10GB/s out, 10 GB/s in
- 25+ GB/s XDR memory interface

## Accelerated Functions

- Signal processing
- Image processing
- Audio resampling
- Noise generation
- Sound oscillation
- Digital filtering
- Curve and surface evaluation
- FFT
- Matrix mathematics
- Vector mathematics
- Game Physics / Physics simulation
- Video compression / decompression
- Surface subdivision
- Transform-light
- Graphics content creation
- Security encryption / decryption
- Pattern matching
- Language parsing
- TCP/IP offload
- Encoding / decoding
- Parallel processing
- Real time processing
- ...

## Target Applications

- Medical imaging / visualization
- Drug discovery
- Petroleum reservoir modeling
- Seismic analysis
- Avionics
- Air traffic control systems
- Radar systems
- Sonar systems
- Training simulation
- Targeting
- Defense and security IT
- Surveillance
- Secure communications
- LAN/MAN Routers
- Network processing
- XML and SSL acceleration
- Voice and pattern recognition
- Video conferencing
- Computational chemistry
- Climate modeling
- Data mining and analysis
- Media server
- Digital content creation
- Digital content distribution
- ....